Please amend the subject application as follows:

IN THE CLAIMS:

Please accept amended claims 1-4 and 13-16 and new claim 22 as follows:

1. (Currently Amended) A method of fabricating a semiconductor device comprising:

forming a first insulating layer on a substrate;

forming an interconnection line ~~over a substrate~~ within the first insulating layer, wherein the interconnection line functions as a first electrode;

forming a [[first]] second insulating layer on the ~~substrate and~~ first insulating layer including the interconnection line;

forming an electrode layer and an oxide layer on the [[first]] second insulating layer;

forming a photoresist pattern on the oxide layer;

etching the oxide layer and the electrode layer to form a second electrode and an oxide layer pattern stacked over the interconnection line, wherein at least the electrode layer is wet-etched; and

removing the photoresist pattern.

2. (Currently Amended) The method of claim 1, wherein the ~~step of forming the~~ interconnection line ~~comprises:~~

~~forming a second insulating layer on the substrate; and~~

~~forming a pattern in the second insulating layer~~ is formed using a damascene technique.

3. (Currently Amended) The method of claim 2, wherein the ~~pattern~~ interconnection line is formed from a copper layer.

4. (Currently Amended) The method of claim 1, wherein the [[first]] second insulating layer is formed of a dielectric layer.

5. (Original) The method of claim 4, wherein the dielectric layer is formed of one of a silicon nitride layer, a silicon carbide layer, a silicon oxycarbide layer and a silicon carbonitride layer.

6. (Original) The method of claim 1, wherein the electrode layer is formed of one of a tantalum layer, a tantalum nitride layer, a titanium layer and a titanium nitride layer.

7. (Original) The method of claim 1, wherein etching is performed using a mixture of hydrofluoric acid and nitric acid.

8. (Original) The method of claim 1, wherein the electrode layer is formed of one of a tungsten layer and a tungsten nitride layer.

9. (Original) The method of claim 1, wherein the oxide layer is one of wet-etched and dry-etched, and the electrode layer is wet-etched using hydrogen peroxide.

10. (Original) The method of claim 1, further comprising using the photoresist pattern as an etching mask.

11. (Original) The method of claim 1, wherein the electrode layer is formed from metal.

12. (Original) The method of claim 1, wherein the interconnection line is formed from metal.

13. (Currently Amended) A method of fabricating a semiconductor device comprising:

forming a first insulating layer on a substrate;

forming an interconnection line ~~over a substrate~~ within the first insulating layer, wherein the interconnection line functions as a first electrode;

forming [[an]] a second insulating layer on the ~~substrate and~~ first insulating layer including the interconnection line;

forming an electrode layer on the second insulating layer;

forming a photoresist pattern on the electrode layer; and

wet-etching the electrode layer to form a second electrode.

14. (Original) The method of claim 13, wherein the interconnection line is formed from metal.

15. (Currently Amended) The method of claim 13, wherein the ~~insulating layer~~ interconnection line is formed from ~~a dielectric layer~~ copper using a damascene process.

16. (Currently Amended) The method of claim [[15]] 13, wherein the second insulating layer is a dielectric layer [[is]] formed of one of a silicon nitride layer, a silicon carbide layer, a silicon oxycarbide layer and a silicon carbonitride layer.

17. (Original) The method of claim 13, wherein the electrode layer is formed of one of a tantalum layer, a tantalum nitride layer, a titanium layer, a titanium nitride layer, a tungsten layer and a tungsten nitride layer.

18. (Original) The method of claim 13, wherein the electrode layer is wet-etched using one of hydrogen peroxide and a mixture of hydrofluoric acid and nitric acid.

19. (Original) The method of claim 13, further comprising:

forming an oxide layer on the electrode layer; and

one of wet-etching and dry-etching the oxide layer.

20. (Original) The method of claim 13, further comprising removing the photoresist pattern.

21. (Original) The method of claim 13, wherein the electrode layer is formed from metal.

22. (New) A method of fabricating a metal-insulator-metal capacitor, comprising:

forming an insulating layer on a substrate;

forming an interconnection line within the insulating layer, wherein the interconnection line is a first electrode of the metal-insulator-metal capacitor;

forming a dielectric layer on the insulating layer including the interconnection line;

forming an electrode layer on the dielectric layer;

forming a photoresist pattern on the electrode layer; and

etching the electrode layer using the photoresist pattern as a mask to form a second electrode of the metal-insulator-metal capacitor.